IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of		Docket No.:	**TI-30674**
	Robert B. Staszewski, et al.	Examiner:	**Kinkead**
Serial No.:	**09/695,516**	Art Unit:	**2817**
Filed:	**10/24/00**	Confirm. No.:	**3115**

For: **HYBRID OF PREDICTIVE AND CLOSED-LOOP PHASE DOMAIN DIGITAL PLL ARCHITECTURE**

AMENDMENT - 37 C.F.R. § 1.111

Assistant Commissioner for Patents

Washington, D.C. 20231

CERTIFICATION OF FAX TRANSMITTAL

I hereby certify that the above correspondence is being facsimile transmitted to the United States Patent and Trademark Office on September 17, 2002.

Elizabeth Austin

Dear Sir:

Responsive to the Office Action dated May 22, 2002, please amend the above-identified application, as set forth below.

IN THE CLAIMS – (clean copy):

1. (amended) A digital phase-domain phase-locked loop circuit comprising:

a digitally-controlled oscillator (DCO);

a gain element feeding the DCO and operational to compensate for DCO gain in response t

a digital phase accumulator operational to accumulate DCO generated clock edges.